WHAT IS CLAIMED IS:

1. A LCD driver comprising a capacitor divider connected to row and/or column electrodes of a LCD, said divider comprising a plurality of capacitors that are electrically connected to provide voltage level(s) and power for driving the LCD.

2. The driver of claim 1, said divider comprising two reference nodes and a third node conneccted to the reference nodes through capacitors, wherein the values of the capacitors cause a predetermined bias ratio of voltage levels to be maintained across the capacitors.

3. The driver of claim 1, further comprising a circuit refreshing the voltage level(s) at the third node and one of the two reference nodes.

4. The driver of claim 3, said circuit comprising a switching device that periodically discharges the capacitors and at least one power supply that periodically charges the two nodes to predetermined voltages.

5. The driver of claim 1, further comprising a switching device that connects the capacitors to provide suitable voltage level(s) for driving the LCD.

6. The driver of claim 5, wherein the switching device connects the capacitors so that they are connected in parallel to a power source to charge the capacitors, and connected in series to provide voltage levels for driving the LCD.

7. A LCD driver comprising:

a capacitor divider which comprises a plurality of capacitors; and

a switching device connecting the divider to row and column electrodes of a LCD, to provide suitable IAPT voltage level(s) for driving the electrodes.

8. The driver of claim 7, said divider comprising 2, 3, 4 or 5 capacitors.

9. The driver of claim 8, said divider comprising a first, second, third, fourth and fifth capacitor connected in series between two nodes, wherein the first and second capacitors have substantially the same capacitance and the fourth and fifth capacitors have substantially the same capacitance.

10. The driver of claim 8, wherein said capacitors have substantially the same capacitance.

11. The driver of claim 7, wherein the switching device connects the divider to row and column electrodes of a LCD through four nodes: a first and a second column node and a row scanning node and a row non-scanning node.

12. The driver of claim 11, the divider comprising 5 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first, second, third and fourth connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node.

13. The driver of claim 12, wherein during a first addressing phase, the switching device connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

14. The driver of claim 13, wherein during the first addressing phase, the switching device connects the first column node to the low reference node and the second column node to the second connecting node.

15. The driver of claim 14, wherein during a second addressing phase, the switching device connects the row non-scanning node to the fourth connecting node and the row scanning node to the low reference node.

16. The driver of claim 14, wherein during the second addressing phase, the switching device connects the first column node to the third connecting node and the second column node to the high reference node.

17. The driver of claim 11, the divider comprising 4 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first, second and a third connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node.

18. The driver of claim 17, wherein during a first addressing phase, the switching device connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

19. The driver of claim 18, wherein during the first addressing phase, the switching device connects the first column node to the low reference node and the second column node to the second connecting node.

20. The driver of claim 18, wherein during a second addressing phase, the switching device connects the row non-scanning node to the third connecting node and the row scanning node to the low reference node.

21. The driver of claim 18, wherein during the second addressing phase, the switching device connects the first column node to the second connecting node and the second column node to the high reference node.

22. The driver of claim 11, the divider comprising 3 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first and a second connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node.

23. The driver of claim 22, wherein during a first addressing phase, the switching device connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

24. The driver of claim 23, wherein during the first addressing phase, the switching device connects the first column node to the low reference node and the second column node to the second connecting node.

25. The driver of claim 24, wherein during a second addressing phase, the switching device connects the row non-scanning node to the second connecting node and the row scanning node to the low reference node.

26. The driver of claim 24, wherein during the second addressing phase, the switching device connects the first column node to the first connecting node and the second column node to the high reference node.

27. A method for driving a LCD comprising:

providing a capacitor divider which comprises a plurality of capacitors; and

connecting the divider to row and column electrodes of a LCD, to provide suitable voltage level(s) for driving the electrodes.

28. The method of claim 27, wherein the connecting causes the divider to provide suitable IAPT voltage level(s) for driving the electrodes.

29. The method of claim 27, said divider comprising two reference nodes and a third node connected to the reference nodes through capacitors, said method further comprising refreshing the voltage level(s) at the third node and one of the two reference nodes.

30. The method of claim 29, said refreshing comprising periodically discharging the capacitors and periodically charging the two nodes to predetermined voltages.

31. The method of claim 27, wherein the connecting connects the capacitors in parallel to a power source to charge the capacitors, and connects the capacitors in series to provide voltage levels for driving the LCD.

32. The method of claim 27, wherein the connecting connects the divider to row and column electrodes of a LCD through four nodes: a first and a second column node and a row scanning node and a row non-scanning node.

33. The method of claim 32, the divider comprising 5 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first, second, third and fourth connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node, wherein during a first addressing phase, the connecting connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

34. The method of claim 33, wherein during the first addressing phase, the connecting connects the first column node to the low reference node and the second column node to the second connecting node.

35. The method of claim 33, wherein during a second addressing phase, the connecting connects the row non-scanning node to the fourth connecting node and the row scanning node to the low reference node.

36. The method of claim 35, wherein during the second addressing phase, the connecting connects the first column node to the third connecting node and the second column node to the high reference node.

37. The method of claim 32, the divider comprising 4 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first, second and a third connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node, wherein during a first addressing phase, the connecting connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

38. The method of claim 37, wherein during the first addressing phase, the connecting connects the first column node to the low reference node and the second column node to the second connecting node.

39. The method of claim 37, wherein during a second addressing phase, the connecting connects the row non-scanning node to the third connecting node and the row scanning node to the low reference node.

40. The method of claim 39, wherein during the second addressing phase, the switching device connects the first column node to the second connecting node and the second column node to the high reference node.

41. The method of claim 32, the divider comprising 3 capacitors connected in series between a low and a high reference node, and to one another through a sequence of a first and a second connecting node at ascending electrical potentials, wherein the high reference node is at a higher electrical potential than the low reference node, wherein during a first addressing phase, the connecting connects the row non-scanning node to the first connecting node and the row scanning node to the high reference node.

42. The method of claim 41, wherein during the first addressing phase, the connecting connects the first column node to the low reference node and the second column node to the second connecting node.

43. The method of claim 41, wherein during a second addressing phase, the connecting connects the row non-scanning node to the second connecting node and the row scanning node to the low reference node.

44. The method of claim 43, wherein during the second addressing phase, the connecting connects the first column node to the first connecting node and the second column node to the high reference node.